IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	Group Art Unit: 2818
ELIYAHOU HARARI, ROBERT D. NORMAN and SANJAY MEHROTRA	Examiner: A. Tran
Serial No.: 09/129,675	
Filed: August 5, 1998	
For: FLASH EEPROM SYSTEM	San Francisco, California

Assistant Commissioner for Patents
Washington, D.C. 20231

By Express Mail No.: EM552309799US
Dated: October 29, 1999

SECOND VOLUNTARY AMENDMENT

Sir:

Please add the following new claims 100-111 to the above-captioned patent application:

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--100. A method for programming a non-volatile semiconductor memory device including a plurality of memory cells, a word line a, plurality of bit lines, and a plurality of data latch circuits, in which said plurality of memory cells are coupled to the word line and are coupled to said plurality of data latch circuits through said plurality of bit lines, the method comprising the following steps of:

storing data of a first logic level or a second logic level into said plurality of data latch circuits;

applying a programming voltage to said word line;

applying a first level voltage corresponding to the first logic level or a second level voltage corresponding to the second logic level to said bit lines in accordance with the level of the data stored in said plurality of data latch circuits, wherein said first level voltage promotes